UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/976,731	10/12/2001	Leilei Song	3	2455

7590 01/22/2004

Ryan, Mason & Lewis, LLP
Suite 205
1300 Post Road
Fairfield, CT 06430

EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 01/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/976,731	SONG, LEILEI	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *11-24 and 27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,25 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-10, 25 and 26, drawn to Error Count for Reducing Power Consumption, classified in class 714, subclass 708.

   II. Claims 11-24, drawn to A Key Equation Determining Device whereby New Values of Polynomial Coefficients Are Calculated, classified in class 714, subclass 781.

   III. Claim 27, drawn to An Encoder for Parallel Generation of Parity, classified in class 714, subclass 757.

The inventions are distinct, each from the other because of the following reasons: Inventions Group I, Error Count for Reducing Power Consumption, and Group II, A Key Equation Determining Device whereby New Values of Polynomial Coefficients Are Calculated, are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination, Group I, Error Count for Reducing Power Consumption, as claimed does not require the particulars of the subcombination, Group II, A Key Equation Determining Device whereby New Values of Polynomial Coefficients

Are Calculated, as claimed because the combination does not require the calculation of new values of polynomial coefficients. The subcombination has separate utility such as in an iterative decoding process whereby the calculation of new values of polynomial coefficients is required.

Inventions Group I, Error Count for Reducing Power Consumption, and Group III, An Encoder for Parallel Generation of Parity, are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I, Error Count for Reducing Power Consumption, has separate utility such as in a receiver. In the instant case, invention Group III, An Encoder for Parallel Generation of Parity, has separate utility such as in a transmitter. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II and vice a versa, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group III and vice a versa, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group II is not required for Group III and vice a versa, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Robert J. Mauri on 13 January 2004 a provisional election was made with traverse to prosecute the invention of Group I, claims 1-10, 25 and 26. Affirmation of this election must be made by applicant in replying to this Office action. Claims 11-24 and 27 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: '1375' on page 25 of the specification. A proposed drawing correction or

corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: '999' in Figure 9; '1052' in Figure 10(b); and '1400' in Figure 14. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 5 and 6 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 5 recites, "placing a predetermined state into each of the intermediate polynomials, the predetermined state selected to reduce switching of the calculation

circuit". Nowhere does the Applicant teach placing a predetermined state into each of the intermediate polynomials, the predetermined state selected to reduce switching of the calculation circuit.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. R(x), F(x) and Q(x) are undefined in claim 4, which renders the claim indefinite

6. Claims 5 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 5 recites, "placing a predetermined state into each of the intermediate polynomials, the predetermined state selected to reduce switching of the calculation circuit". A polynomial is a mathematical expression and a state cannot be placed into a polynomial.

7. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP

§ 2172.01. The omitted structural cooperative relationships are: the relationship between R(x), F(x) and Q(x).

8. Claims 5 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Claim 5 recites, "placing a predetermined state into each of the intermediate polynomials, the predetermined state selected to reduce switching of the calculation circuit". The omitted structural cooperative relationships are: the relationship between a polynomial and a predetermined state.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Yang, Honda et al. (US 6606727 B1, hereafter referred to as Yang).

Examiner's Comment.

MPEP § 2131.01 states "To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991). The Examiner introduces Ott, Stefan (US 6182264 B1) and Wasada, Langford M. (US 5970075 A) as teaching references for that which is inherent in the Yang patent. More specifically Yang teaches an iterative algorithm comprising various processing steps and Ott teaches unnecessary error correction wastes processor capacity in the receiving and transmitting devices and signal processing effort is wasted encoding and decoding error correction information, which in turn, needlessly slows the performance of the system and increases power consumption (col. 2, lines 10-13, Ott), that is, decreased error correction processing reduces power consumption just as increased error correction processing increases power consumption. In addition, Yang teaches the use of identification of uncorrectable errors for Reed-Solomon codes (see Abstract, Yang) and Wasada teaches the well-known relationship between uncorrectable errors and the error location polynomial, that is; if the degree of the error locator polynomial is greater than the maximum number of correctable errors for a Reed-Solomon block of code, then the block is uncorrectable (col. 9, lines 29-33, Wasada).

35 U.S.C. 102(e) rejection of claims 1 and 25.

Yang teaches a method performed in an error correction system and a decoder for implementing the method (See Figures 1 and 5 in Yang), the method comprising the steps of: determining if an actual number of errors is less than a maximum error correction capability (in Step 67 in Figure 5 of Yang, decoding is completed and after Step 67 a test for uncorrectable errors is performed and if it is determined that no uncorrectable errors exist, the processing is terminated, see col. 8, lines 45-46 in Yang; Note: an uncorrectable error is an error that exceeds the maximum error correction capability of an error correction code; hence processing in Figure 5 of Yang is stopped if it is determined that an actual number of errors is less than a maximum error correction capability); and reducing power consumption in a decoder of the error correction system when the actual number of errors is less than the maximum error correction capability (Note: a step for early termination of error correction processing when it is determined that no uncorrectable error exist, i.e. an actual number of errors is less than a maximum error correction capability, is a step for reducing power consumption in a decoder, see previous Examiner's Comment regarding the Ott patent).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yang, Honda et al. (US 6606727 B1, hereafter referred to as Yang) in view of the Applicant's Admitted Prior Art.

35 U.S.C. 103(a) rejection of claim 2.

Yang, substantially teaches the claimed invention described in claims 1 and 25 (as rejected above).

However Yang, does not explicitly teach the specific use of gating clocks.

The Applicant admits in lines 26 and 27 of page 15 that clock gating is a well known in the art. The Examiner asserts that Yang teaches reducing power consumption of error decoding circuitry when errors are less then a maximum error correction capability. It would be an obvious Engineering design choice to use a circuit technique well-know in the art based on available circuitry and available circuit techniques for carrying out the circuit design requirements.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yang with the teachings of Applicant's Admitted Prior Art

by including use of gating clocks. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of gating clocks would have provided the opportunity to implement control circuitry for the method taught in the Yang patent whereby power consumption of error decoding circuitry is reduced when errors are less then a maximum error correction capability.

11. Claims 3-6 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang, Honda et al. (US 6606727 B1, hereafter referred to as Yang).

35 U.S.C. 103(a) rejection of claim 3.

Yang, substantially teaches the claimed invention described in claim 1 (as rejected above).

However Yang, does not explicitly teach the specific use of a step for **determining if a degree of at least one of the intermediate polynomials is less than a predetermined degree** for use in detecting an uncorrectable error.

The Examiner asserts that that Yang teaches, in Step 67 in Figure 5 of Yang, decoding is completed and after Step 67 a test for uncorrectable errors is performed and if it is determined that no uncorrectable errors exist, the processing is terminated (see col. 8, lines 45-46; Note: an uncorrectable error is an error that exceeds the maximum error correction capability of an error correction code; hence processing in Figure 5 of Yang is stopped if it is determined that an actual number of errors is less than a maximum error

correction capability). The Examiner asserts that it is well-known in the art that if the degree of the error locator polynomial is greater than the maximum number of correctable errors for a Reed-Solomon block of code, then the block is uncorrectable (see above Examiner's Comment regarding the Wasada reference; Note: an error locator polynomial is an intermediate polynomial since it is only used in intermediate steps for error correction and is not a final result); hence if the degree of the error locator polynomial is less than the maximum number of correctable errors the block is correctable. Therefore it would be obvious to use that which is well-known in the art for determining an uncorrectable error to carry out the required step in the Yang patent of determining whether a block of Reed-Solomon code is correctable or not.
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Yang by including an additional step of for determining if a degree of at least one of the intermediate polynomials is less than a predetermined degree. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that for determining if a degree of at least one of the intermediate polynomials is less than a predetermined degree would have provided the opportunity to carry out the required step in the Yang patent of determining whether a block of Reed-Solomon code is correctable or not (see col. 8, lines 45-46 in Yang).

35 U.S.C. 103(a) rejection of claims 4-6.

If R(x) is an error location polynomial then a degree of either R(x) or Q(x) is less than a predetermined degree whenever R(x) is less than a predetermined degree.

35 U.S.C. 103(a) rejection of claim 26.

Yang teaches a method performed in an error correction system and a decoder for implementing the method (See Figures 1 and 5 in Yang), the method comprising the steps of: determining if an actual number of errors is less than a maximum error correction capability (in Step 67 in Figure 5 of Yang, decoding is completed and after Step 67 a test for uncorrectable errors is performed and if it is determined that no uncorrectable errors exist, the processing is terminated, see col. 8, lines 45-46 in Yang; Note: an uncorrectable error is an error that exceeds the maximum error correction capability of an error correction code; hence processing in Figure 5 of Yang is stopped if it is determined that an actual number of errors is less than a maximum error correction capability); and reducing power consumption in a decoder of the error correction system when the actual number of errors is less than the maximum error correction capability (Note: a step for early termination of error correction processing when it is determined that no uncorrectable error exist, i.e. an actual number of errors is less than a maximum error correction capability, is a step for reducing power consumption in a decoder, see previous Examiner's Comment regarding the Ott patent).

However Yang, does not explicitly teach the specific use of an integrated circuit comprising a decoder.

The Examiner asserts that it would have been an obvious Engineering Design Choice to implement a decoder as part of an integrated circuit since hardware provides a considerable speed up over software methods for implementing decoders. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Yang by including use of an integrated circuit comprising a decoder. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of an integrated circuit comprising a decoder would have provided considerable speed up over software methods for implementing decoders.

12. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang, Honda et al. (US 6606727 B1, hereafter referred to as Yang) in view of Wasada, Langford M. (US 5970075 A).

35 U.S.C. 103(a) rejection of claims 7 and 8.

Yang, substantially teaches the claimed invention described in claim 1 (as rejected above). In addition, Yang teaches determining a plurality of syndromes (col. 4, lines 39-42 of Yang teach that partial syndromes are computed for determining uncorrectable errors; Note: partial syndromes are syndromes for codewords without extended checkbits and are used in the error correcting process, if it is determined that no uncorrectable errors exist, see Step 66 in Figure 5 of Yang).

However Yang, does not explicitly teach the specific use of reducing power consumption of the decoder of the error correction system when all of the syndromes have the predetermined value.

Wasada, in an analogous art, teaches reducing power consumption of the decoder by bypassing error correction of the error correction system when all of the syndromes have the predetermined value of zero in Step 303 of Figure 3 in Wasada (Note: if the syndromes have the predetermined value of zero in Step 303 of Figure 3 in Wasada, key equation Steps 307-319 are bypassed).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yang with the teachings of Wasada by including an additional step of reducing power consumption of the decoder of the error correction system when all of the syndromes have the predetermined value. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that reducing power consumption of the decoder of the error correction system when all of the syndromes have the predetermined value would have provided the opportunity to bypass error correction processing steps (Note: if the syndromes have the predetermined value of zero in Step 303 of Figure 3 in Wasada, key equation Steps 307-319 are bypassed).

13. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang, Honda et al. (US 6606727 B1, hereafter referred to as Yang) and Wasada, Langford M. (US 5970075 A) in view of Chen, Yen-Hao (US 6571368 B1).

35 U.S.C. 103(a) rejection of claim 9.

Yang and Wasada substantially teach the claimed invention described in claims 1, 7 and 8 (as rejected above). In addition, Yang and Wasada teach the steps of providing a key equation solving steps in the decoding (Steps 307-319 in Wasada are key equation steps), and providing a plurality of syndromes, and wherein the step of reducing power consumption of the decoder of the error correction system when all syndromes have the predetermined value further comprises the step of not enabling the key equation solving device when all of the syndromes have the predetermined value (Note: if the syndromes have the predetermined value of zero in Step 303 of Figure 3 in Wasada, key equation Steps 307-319 are bypassed).

However Yang and Wasada do not explicitly teach the specific use of the hardware required to implement the method in the Yang and Wasada patents such as syndrome generators and key equation solvers.

Chen, in an analogous art, teaches the specific use of the hardware required to implement the method in the Yang and Wasada patents such as syndrome generators and key equation solvers which are required for use in decoding Reed-Solomon code. In Figure 7 of Chen, Chen teaches a plurality of Syndrome generators 600-605 coupled to key equation solvers 610-615. One of ordinary skill in the art at the time the invention

was made would have been highly motivated to combine the Yang and Wasada patents with the Chen patent since Chen teaches in Chen's Abstract that such a design as taught in Figure 7 of Chen would reduce complexity and computation times. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yang and Wasada with the teachings of Chen by including use of the hardware required to implement the method in the Yang and Wasada patents such as syndrome generators and key equation solvers. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of the hardware required to implement the method in the Yang and Wasada patents such as syndrome generators and key equation solvers would have provided the opportunity to reduce complexity and computation times (see Chen's Abstract).

35 U.S.C. 103(a) rejection of claim 10.

In Step 303 of Figure 3 in Wasada and Figure 5 of Yang, at least one error polynomial is calculated when at least one syndrome does not have the predetermined value.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Zook, Christopher P. (US 6272659 B1) teaches a method and apparatus for correcting a multi-dimensional code, such as a product code, by adjusting the correction power during the iterative passes to minimize miscorrections. Weng, Lih-

Jyh (US 4866716 A) teaches decoding of Bose-Chaudhuri-Hocquenghem (BCH) error correction codes, including Reed-Solomon error correction codes. Hallberg, Bryan Severt (US 6640327 B1) teaches a method and apparatus for performing error detection and correction using cyclic codes. Havemose, Allan (US 5412667 A) teaches a Reed-Solomon decoder which performs a reduced number of computations compared to conventional decoding methods. Bi, Qi (US 5483236 A) teaches decoders capable of bit-error correction in stored or transmitted digital information and in particular to decoders of information encoded with BCH or Reed-Solomon code.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.

Joseph D. Torres, PhD
Art Unit 2133